Attia, John Okyere. “Operational Amplifiers.”
Electronics and Circuit Analysis using MATLAB.
Ed. John Okyere Attia
Boca Raton: CRC Press LLC, 1999

CHAPTER ELEVEN

OPERATIONAL AMPLIFIERS

The operational amplifier (Op Amp) is one of the versatile electronic circuits. It can be used to perform the basic mathematical operations: addition, subtraction, multiplication, and division. They can also be used to do integration and differentiation. There are several electronic circuits that use an op amp as an integral element. Some of these circuits are amplifiers, filters, oscillators, and flip-flops. In this chapter, the basic properties of op amps will be discussed. The non-ideal characteristics of the op amp will be illustrated, whenever possible, with example problems solved using MATLAB.

11.1 PROPERTIES OF THE OP AMP

The op amp, from a signal point of view, is a three-terminal device: two inputs and one output. Its symbol is shown in Figure 11.1. The inverting input is designated by the '-' sign and non-inverting input by the '+' sign.

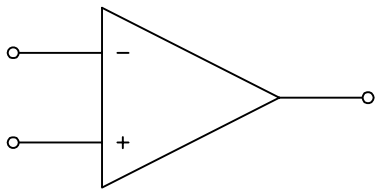


Figure 11.1 Op Amp Circuit Symbol

An ideal op amp has an equivalent circuit shown in Figure 11.2. It is a difference amplifier, with output equal to the amplified difference of the two inputs.

An ideal op amp has the following properties:

- infinite input resistance,
- zero output resistance,
- zero offset voltage,
- infinite frequency response and
- infinite common-mode rejection ratio,
- infinite open-loop gain, A.

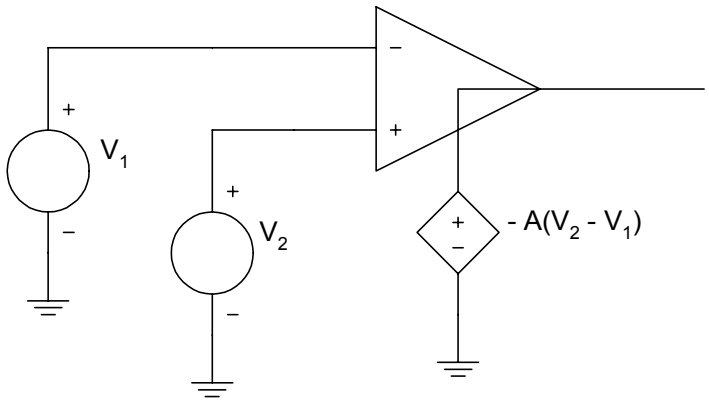


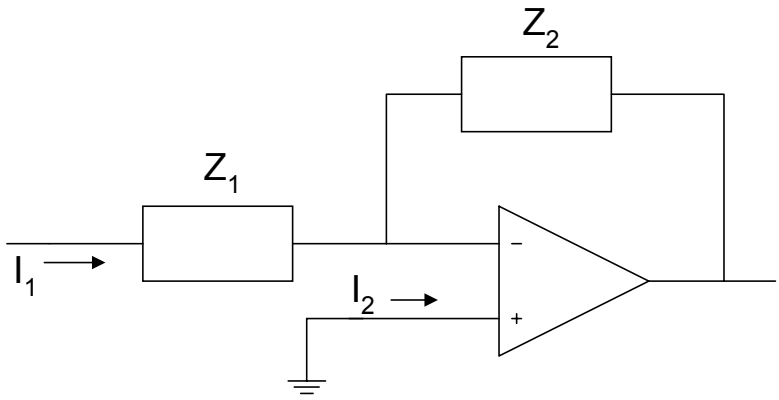
Figure 11.2 Equivalent Circuit of an Ideal Op Amp

A practical op amp will have large but finite open-loop gain in the range from 10^5 to 10^9. It also has a very large input resistance 10^6 to 10^{10} ohms. The output resistance might be in the range of 50 to 125 ohms. The offset voltage is small but finite and the frequency response will deviate considerably from the infinite frequency response. The common-mode rejection ratio is not infinite but finite. Table 11.1 shows the properties of the general purpose 741 op amp.

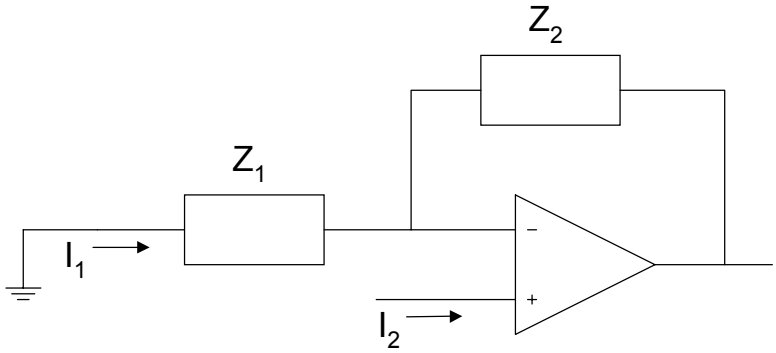
Table 11.1
Properties of 741 Op Amp

Property	**Value (Typical)**
Open Loop Gain	$2x10^5$
Input resistance	2.0 M
Output resistance	75 Ω
Offset voltage	1 mV
Input bias current	30 nA
Unity-gain bandwidth	1 MHz
Common-mode rejection ratio	95 dB
Slew rate	0.7 V/μV

Whenever there is a connection from the output of the op amp to the inverting input as shown in Figure 11.3, we have a negative feedback connection



(a)



(b)

Figure 11.3 Negative Feedback Connections for Op Amp
(a) Inverting (b) Non-inverting configurations

With negative feedback and finite output voltage, Figure 11.2 shows that

$$V_O = A\left(V_2 - V_1\right) \tag{11.1}$$

Since the open-loop gain is very large,

$$\left(V_2 - V_1\right) = \frac{V_O}{A} \cong 0 \tag{11.2}$$

Equation (11.2) implies that the two input voltages are also equal. This condition is termed the concept of the virtual short circuit. In addition, because of the large input resistance of the op amp, the latter is assumed to take no current for most calculations.

11.2 INVERTING CONFIGURATION

An op amp circuit connected in an inverted closed loop configuration is shown in Figure 11.4.

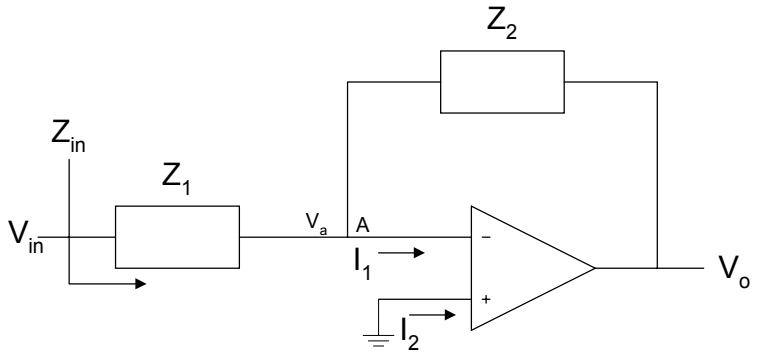


Figure 11.4 Inverting Configuration of an Op Amp

Using nodal analysis at node A, we have

$$\frac{V_a - V_{in}}{Z_1} + \frac{V_a - V_O}{Z_2} + I_1 = 0 \tag{11.3}$$

From the concept of a virtual short circuit,

$$V_a = V_b = 0 \tag{11.4}$$

and because of the large input resistance, $I_1 = 0$. Thus, Equation (11.3) simplifies to

$$\frac{V_O}{V_{IN}} = -\frac{Z_2}{Z_1} \tag{11.5}$$

The minus sign implies that V_{IN} and V_0 are out of phase by 180°. The input impedance, Z_{IN}, is given as

$$Z_{IN} = \frac{V_{IN}}{I_1} = Z_1 \tag{11.6}$$

If $Z_1 = R_1$ and $Z_2 = R_2$, we have an inverting amplifier shown in Figure 11.5.

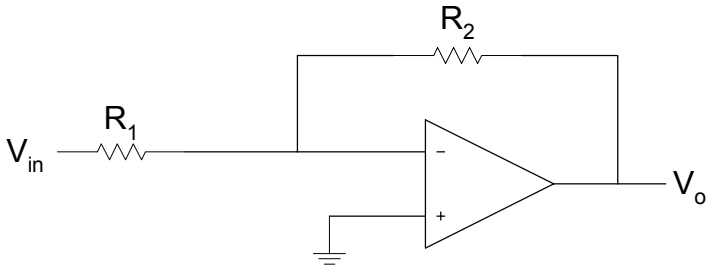


Figure 11.5 Inverting Amplifier

The closed-loop gain of the amplifier is

$$\frac{V_O}{V_{IN}} = -\frac{R_2}{R_1} \tag{11.7}$$

and the input resistance is R_1. Normally, $R_2 > R_1$ such that $|V_0| > |V_{IN}|$. With the assumptions of very large open-loop gain and high input resistance, the closed-loop gain of the inverting amplifier depends on the external components R_1, R_2, and is independent of the open-loop gain.

For Figure 11.4, if $Z_1 = R_1$ and $Z_2 = \frac{1}{jwC}$, we obtain an integrator circuit shown in Figure 11.6. The closed-loop gain of the integrator is

$$\frac{V_O}{V_{IN}} = -\frac{1}{jwCR_1} \tag{11.8}$$

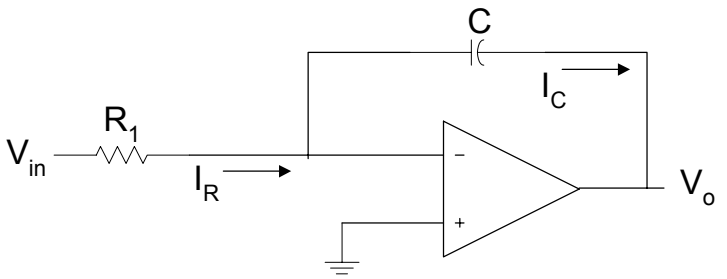


Figure 11.6 Op Amp Inverting Integrator

In the time domain

$$\frac{V_{IN}}{R_1} = I_R \text{ and } I_C = -C\frac{dV_O}{dt} \tag{11.9}$$

Since $I_R = I_C$

$$V_O(t) = -\frac{1}{R_1 C}\int_0^t V_{IN}(t)d\tau + V_O(0) \tag{11.10}$$

The above circuit is termed the Miller integrator. The integrating time constant is CR_1. It behaves as a lowpass filter, passing low frequencies and attenuating high frequencies. However, at dc the capacitor becomes open circuited and there is no longer a negative feedback from the output to the input. The output voltage then saturates. To provide finite closed-loop gain at dc, a resistance R_2 is connected in parallel with the capacitor. The circuit is shown in Figure 11.7. The resistance R_2 is chosen such that R_2 is greater than R.

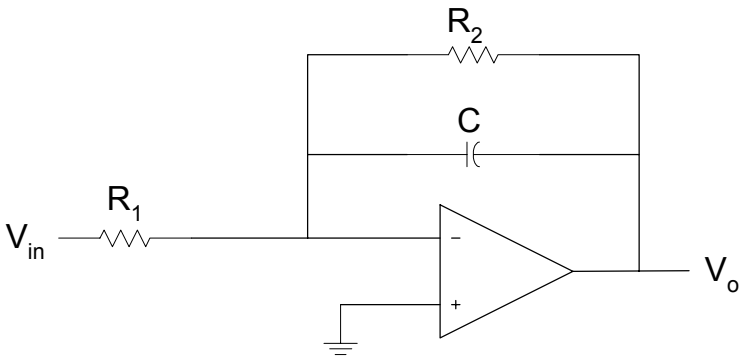


Figure 11.7 Miller Integrator with Finite Closed Loop Gain at DC

For Figure 11.4, if $Z_1 = \frac{1}{jwC}$ and $Z_2 = R$, we obtain a differentiator circuit shown in Figure 11.8. From Equation (11.5), the closed-loop gain of the differentiator is

$$\frac{V_O}{V_{IN}} = -jwCR \tag{11.11}$$

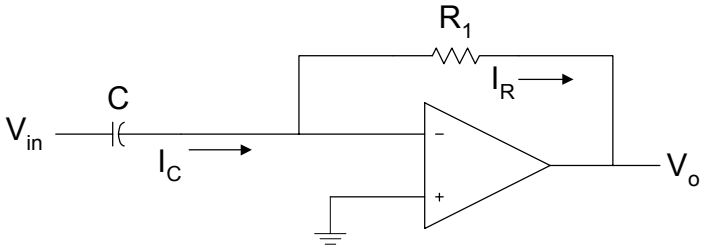


Figure 11.8 Op Amp Differentiator Circuit

In the time domain

$$I_C = C\frac{dV_{IN}}{dt}\text{, and } V_O(t) = -I_R R \tag{11.12}$$

Since

$$I_C(t) = I_R(t)$$

we have

$$V_O(t) = -CR\frac{dV_{IN}(t)}{dt} \tag{11.13}$$

Differentiator circuits will differentiate input signals. This implies that if an input signal is rapidly changing, the output of the differentiator circuit will appear " spike-like."

The inverting configuration can be modified to produce a weighted summer. This circuit is shown in Figure 11.9.

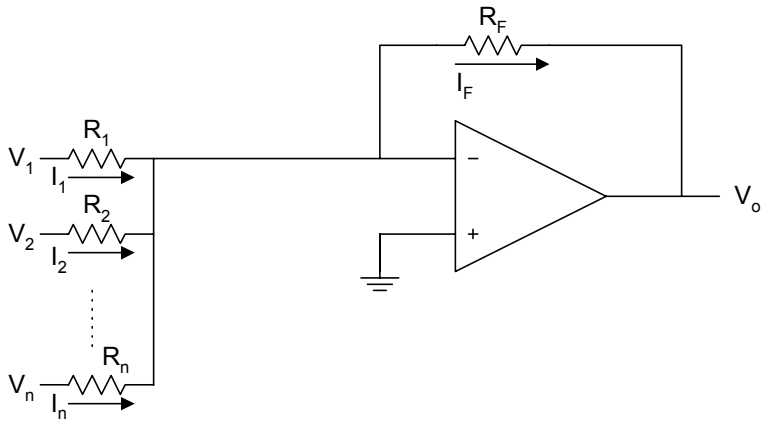


Figure 11.9 Weighted Summer Circuit

From Figure 11.9

$$I_1 = \frac{V_1}{R_1}, \quad I_2 = \frac{V_2}{R_2}, \quad \ldots\ldots, \quad I_n = \frac{V_n}{R_n} \tag{11.14}$$

also

$$I_F = I_1 + I_2 + \ldots\ldots I_N \tag{11.15}$$

$$V_O = -I_F R_F \tag{11.16}$$

Substituting Equations (11.14) and (11.15) into Equation (11.16) we have

$$V_O = -\left(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \ldots\ldots \frac{R_F}{R_N} V_N \right) \tag{11.17}$$

The frequency response of Miller integrator, with finite closed-loop gain at dc, is obtained in the following example.

Example 11.1

For Figure 11.7, (a) Derive the expression for the transfer function $\frac{V_o}{V_{in}}(jw)$.

(b) If C = 1 nF and R_1 = 2KΩ, plot the magnitude response for R_2 equal to (i) 100 KΩ, (ii) 300KΩ, and (iii) 500KΩ.

Solution

$$Z_2 = R_2 \| \frac{1}{sC_2} = \frac{R_2}{1 + sC_2 R_2} \tag{11.18}$$

$$Z_1 = R_1 \tag{11.19}$$

$$\frac{V_o}{V_{in}}(s) = \frac{-R_2 / R_1}{1 + sC_2 R_2} \tag{11.20}$$

$$\frac{V_o}{V_{in}}(s) = \frac{-1 / C_2 R_1}{s + 1 / C_2 R_2} \tag{11.21}$$

MATLAB Script

```
% Frequency response of lowpass circuit
c = 1e-9; r1 = 2e3;
r2 = [100e3, 300e3, 500e3];
n1 = -1/(c*r1); d1 = 1/(c*r2(1));
num1 = [n1]; den1 = [1 d1];
w = logspace(-2,6);
h1 = freqs(num1,den1,w);
f = w/(2*pi);
```

```
d2 = 1/(c*r2(2)); den2 = [1 d2];
h2 = freqs(num1, den2, w);
d3 = 1/(c*r2(3)); den3 = [1 d3];
h3 = freqs(num1,den3,w);
semilogx(f,abs(h1),'w',f,abs(h2),'w',f,abs(h3),'w')
xlabel('Frequency, Hz')
ylabel('Gain')
axis([1.0e-2,1.0e6,0,260])
text(5.0e-2,35,'R2 = 100 Kilohms')
text(5.0e-2,135,'R2 = 300 Kilohms')
text(5.0e-2,235,'R2 = 500 Kilohms')
title('Integrator Response')
```

Figure 11.10 shows the frequency response of Figure 11.7.

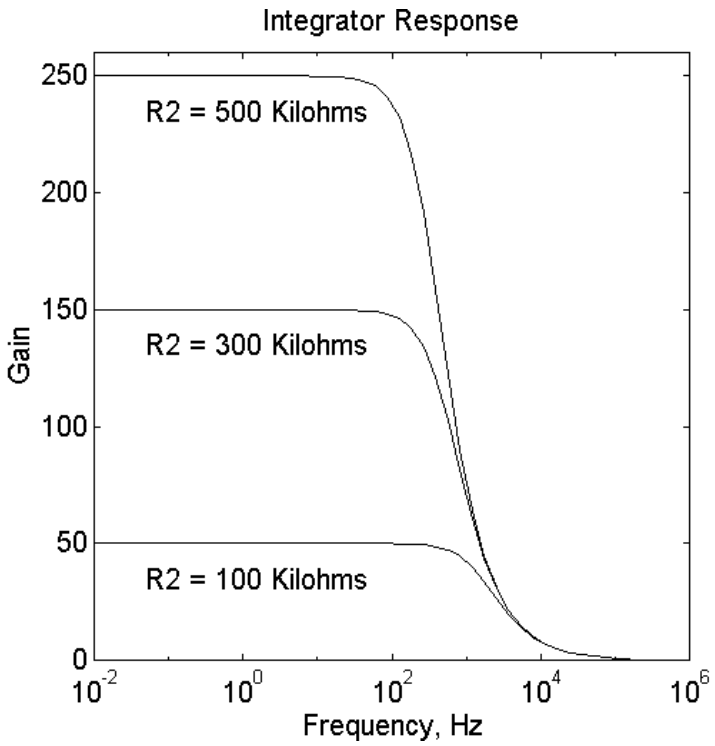


Figure 11.10 Frequency Response of Miller Integrator with Finite Closed-Loop Gain at DC

11.3 NON-INVERTING CONFIGURATION

An op amp connected in a non-inverting configuration is shown in Figure 11.11.

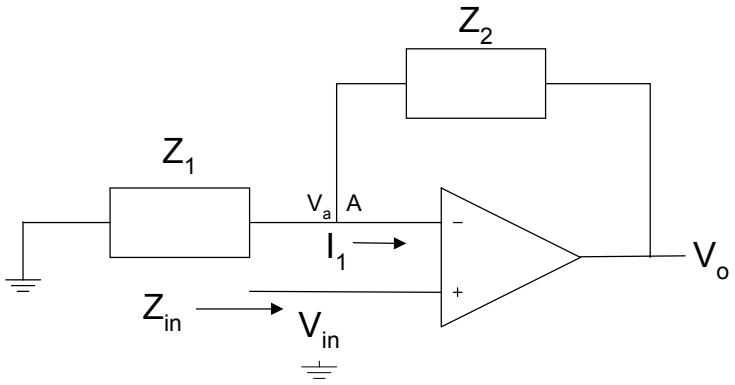


Figure 11.11 Non-Inverting Configuration

Using nodal analysis at node A

$$\frac{V_a}{Z_1} + \frac{V_a - V_O}{Z_2} + I_1 = 0 \tag{11.22}$$

From the concept of a virtual short circuit,

$$V_{IN} = V_a \tag{11.23}$$

and because of the large input resistance ($i_1 = 0$), Equation (11.22) simplifies to

$$\frac{V_O}{V_{IN}} = 1 + \frac{Z_2}{Z_1} \tag{11.24}$$

The gain of the inverting amplifier is positive. The input impedance of the amplifier Z_{IN} approaches infinity, since the current that flows into the positive input of the op-amp is almost zero.

If $Z_1 = R_1$ and $Z_2 = R_2$, Figure 11.10 becomes a voltage follower with gain. This is shown in Figure 11.11.

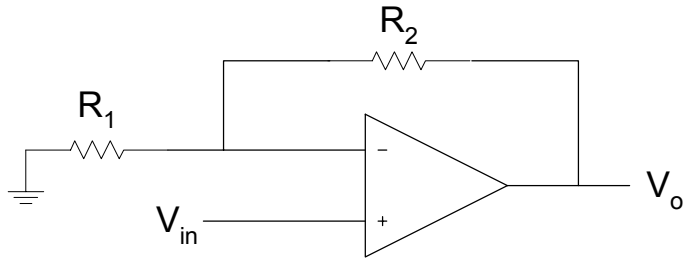


Figure 11.12 Voltage Follower with Gain

The voltage gain is

$$\frac{V_O}{V_{IN}} = \left(1 + \frac{R_2}{R_1}\right) \tag{11.25}$$

The zero, poles and the frequency response of a non-inverting configuration are obtained in Example 11.2.

Example 11.2

For the Figure 11.13 (a) Derive the transfer function. (b) Use MATLAB to find the poles and zeros. (c) Plot the magnitude and phase response, assume that $C_1 = 0.1$uF, $C_2 = 1000\ 0.1$uF, $R_1 = 10$KΩ, and $R_2 = 10\ \Omega$.

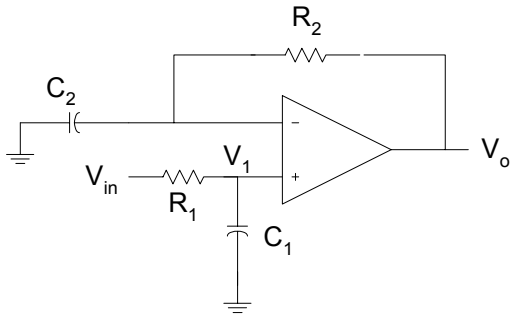


Figure 11.13 Non-inverting Configuration

Solution

Using voltage division

$$\frac{V_1}{V_{IN}}(s) = \frac{1/sC_1}{R_1 + 1/sC_1} \tag{11.26}$$

From Equation (11.24)

$$\frac{V_O}{V_1}(s) = 1 + \frac{R_2}{1/sC_2} \tag{11.27}$$

Using Equations (11.26) and (11.27), we have

$$\frac{V_O}{V_{IN}}(s) = \left(\frac{1 + sC_2R_2}{1 + sC_1R_1}\right) \tag{11.28}$$

The above equation can be rewritten as

$$\frac{V_O}{V_{IN}}(s) = \frac{C_2R_2\left(s + \dfrac{1}{C_2R_2}\right)}{C_1R_1\left(s + \dfrac{1}{C_1R_1}\right)} \tag{11.29}$$

The MATLAB program that can be used to find the poles, zero and plot the frequency response is as follows:

```
diary ex11_2.dat
% Poles and zeros, frequency response of Figure 11.13
%
%
c1 = 1e-7; c2 = 1e-3; r1 = 10e3; r2 = 10;

% poles and zeros
b1 = c2*r2;
a1 = c1*r1;
num = [b1 1];
den = [a1 1];
disp('the zero is')
z = roots(num)
```

```
disp('the poles are')
p = roots(den)

% the frequency response
w = logspace(-2,6);
h = freqs(num,den,w);
gain = 20*log10(abs(h));
f = w/(2*pi);
phase = angle(h)*180/pi;
subplot(211),semilogx(f,gain,'w');
xlabel('Frequency, Hz')
ylabel('Gain, dB')
axis([1.0e-2,1.0e6,0,22])
text(2.0e-2,15,'Magnitude Response')
subplot(212),semilogx(f,phase,'w')
xlabel('Frequency, Hz')
ylabel('Phase')
axis([1.0e-2,1.0e6,0,75])
text(2.0e-2,60,'Phase Response')

diary
```

The results are:

```
the zero is
        z =
             -100

the pole is
        p =
             -1000
```

The magnitude and phase plots are shown in Figure 11.14

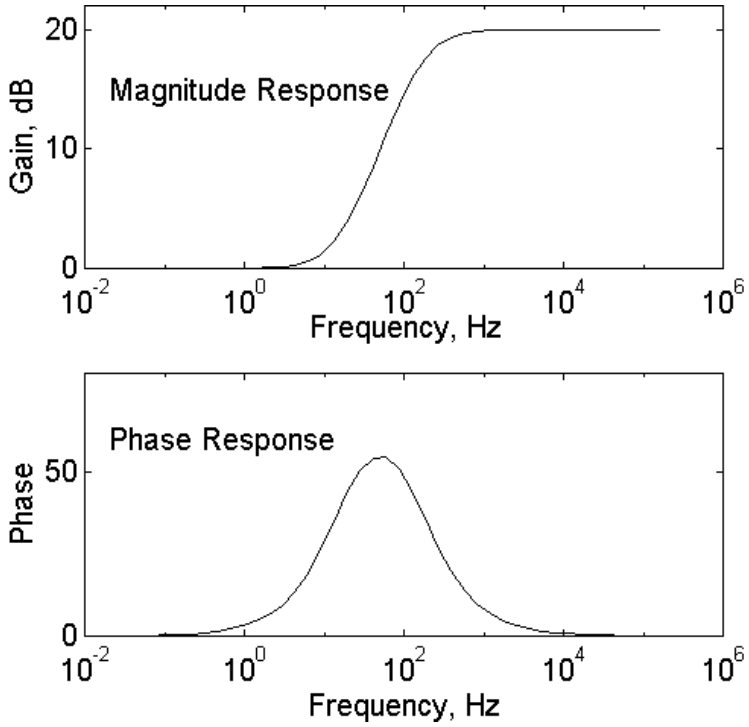


Figure 11.14 Frequency Response of Figure 11.13

11.4 EFFECT OF FINITE OPEN-LOOP GAIN

For the inverting amplifier shown in Figure 11.15, if we assume a finite open-loop gain A, the output voltage V_0 can be expressed as

$$V_O = A\left(V_2 - V_1\right) \tag{11.30}$$

Since $V_2 = 0$,

$$V_1 = -\frac{V_O}{A}$$

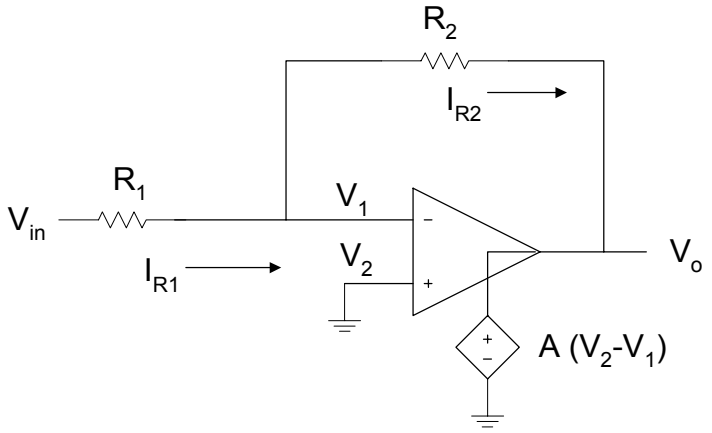


Figure 11.15 Inverter with Finite Open-loop Gain

Because the op amp has a very high input resistance, $i_1 = 0$, we have

$$I_{R1} = I_{R2} \tag{11.31}$$

But

$$I_{R1} = \frac{V_{IN} - V_1}{R_1} = \frac{V_{IN} - V_0/A}{R_1} \tag{11.32}$$

Also

$$V_O = V_1 - I_{R2} R_2 \tag{11.33}$$

Using Equations (11.30), (11.31) and (11.32), Equation (11.33) becomes

$$V_O = -\frac{V_O}{A} - \frac{R_2}{R_1}\left(V_{IN} + V_O/A\right) \tag{11.34}$$

Simplifying Equation (11.34), we get

$$\frac{V_O}{V_{IN}} = -\frac{R_2/R_1}{1 + \left(1 + R_2/R_1\right)/A} \tag{11.35}$$

It should be noted that as the open-loop gain approaches infinity, the closed-loop gain becomes

$$\frac{V_O}{V_{IN}} \cong -\frac{R_2}{R_1}$$

The above expression is identical to Equation (11.7). In addition, from Equation (11.30) , the voltage V_1 goes to zero as the open-loop gain goes to infinity. Furthermore, to minimize the dependence of the closed-loop gain on the value of the open-loop gain, A, we should make

$$\left(1+\frac{R_2}{R_1}\right) << A \qquad (11.36)$$

This is illustrated by the following example.

Example 11.3

In Figure 11.15, R_1 = 500 Ω, and R_2 = 50 KΩ. Plot the closed-loop gain as the open-loop gain increases from 10^2 to 10^8.

Solution

```
% Effect of finite open-loop gain
%
a = logspace(2,8);
r1 = 500; r2 = 50e3; r21 = r2/r1;
g = [];
n = length(a);
for i = 1:n
 g(i) = r21/(1+(1+r21)/a(i));
end
semilogx(a,g,'w')
xlabel('Open loop gain')
ylabel('Closed loop gain')
title('Effect of Finite Open Loop Gain')
axis([1.0e2,1.0e8,40,110])
```

Figure 11.16 shows the characteristics of the closed-loop gain as a function of the open-loop gain.

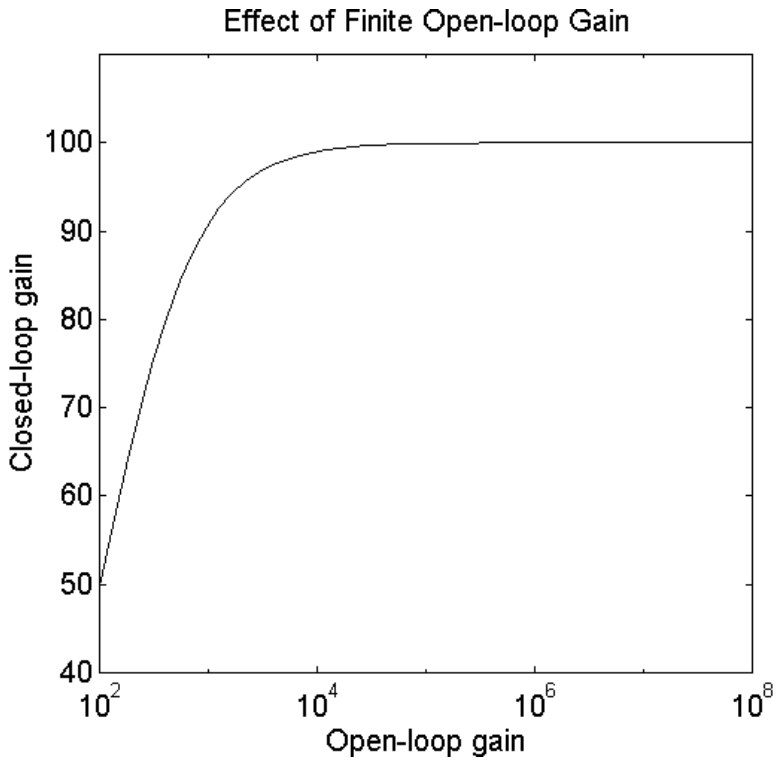


Figure 11.16 Closed-Loop Gain versus Open-Loop Gain

For the voltage follower with gain shown in Figure 11.12, it can be shown that the closed-loop gain of the amplifier with finite open-loop gain is

$$\frac{V_O}{V_{IN}} = -\frac{\left(1 + R_2/R_1\right)}{1 + \left(1 + R_2/R_1\right)/A} \tag{11.37}$$

11.5 FREQUENCY RESPONSE OF OP AMPS

The simplified block diagram of the internal structure of the operational amplifier is shown in Figure 11.17.

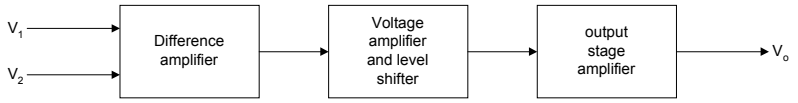


Figure 11.17 Internal Structure of Operational Amplifier

Each of the individual sections of the operational amplifier contains a lowpass RC section, with its corner (pole) frequency. Thus, an op amp will have an open-loop gain with frequency that can be expressed as

$$A(s) = \frac{A_O}{(1 + s/w_1)(1 + s/w_2)(1 + s/w_3)} \tag{11.38}$$

where

$w_1 < w_2 < w_3$

A_O = gain at dc

For most operational amplifiers, w_1 is very small (approx. 20π radians /s) and w_2 might be in the range of 2 to 6 mega-radians/s.

Example 11.4

The constituent parts of an operational amplifier have the following internal characteristics: the pole of the difference amplifier is at 200 Hz and the gain is - 500. The pole of the voltage amplifier and level shifter is 400 KHz and has a gain of 360. The pole of the output stage is 800KHz and the gain is 0.92. Sketch the magnitude response of the operational amplifier open-loop gain.

Solution

The lowpass filter response can be expressed as

$$\frac{V_O}{V_{IN}}(jw) = -\frac{C_{rstage}}{1 + jf/f_p} \tag{11.39}$$

or

$$\frac{V_O}{V_{IN}}(s) = \frac{C_{rstage}}{1 + s/w_p} \tag{11.40}$$

The transfer function of the amplifier is given as

$$A(s) = \frac{-500}{(1 + s/400\pi)} \frac{360}{(1 + s/8\pi 10^5)} \frac{0.92}{(1 + s/1.6\pi 10^6)} \tag{11.41}$$

The above expression simplifies to

$$A(s) = \frac{2.62x10^{21}}{(s + 400\pi)(s + 8\pi 10^5)(s + 1.6\pi 10^6)} \tag{11.42}$$

MATLAB script

```
% Frequency response of op amp
% poles are
p1 = 400*pi; p2 = 8e5*pi; p3 = 1.6e6*pi;
p = [p1 p2 p3];
% zeros
z = [0];
const = 2.62e21;

% convert to poles and zeros  and
% find the frequency response
a3 = 1;
a2 = p1 + p2 + p3;
a1 = p1*p2 + p1*p3 + p2*p3;
a0 = p1*p2*p3;
den = [a3 a2 a1 a0];
num = [const];
w = logspace(1,8);
```

```
h = freqs(num,den,w);
f = w/(2*pi);
g_db = 20*log10(abs(h));

% plot the magnitude response
semilogx(f,g_db)
title('Magnitude response')
xlabel('Frequency, Hz')
ylabel('Gain, dB')
```

The frequency response of the operational amplifier is shown in Figure 11.18.

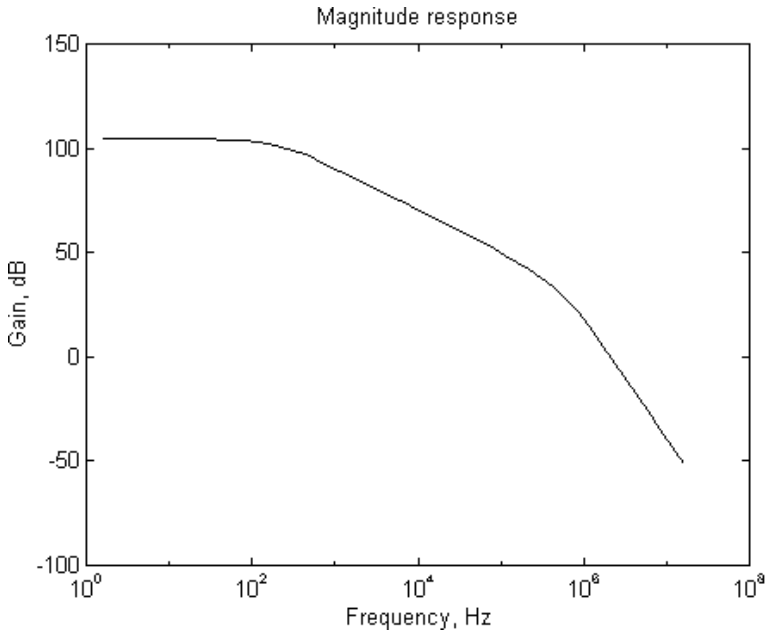


Figure 11.18 Open-Loop Gain Characteristics of an Op Amp

For an internally compensated op amp, there is a capacitor included on the IC chip. This causes the op amp to have a single pole lowpass response. The process of making one pole dominant in the open-loop gain characteristics is called frequency compensation, and the latter is done to ensure the stability of the op amp. For an internally compensated op amp, the open-loop gain $A(s)$ can be written as

$$A(s) = \frac{A_O}{\left(1 + s/w_b\right)} \tag{11.43}$$

where

A_0 is dc open-loop gain

w_b is break frequency.

For the 741 op amp, $A_0 = 10^5$ and $w_b = 20\ \pi$ radians/s. At physical frequencies $s = jw$, Equation (11.43) becomes

$$A(jw) = \frac{A_O}{\left(1 + jw/w_b\right)} \tag{11.44}$$

For frequencies $w > w_b$, Equation (11.44) can be approximated by

$$A(jw) = \frac{A_O w_b}{jw} \tag{11.45}$$

The unity gain bandwidth, w_t (the frequency at which the gain goes to unity), is given as

$$w_t = A_O w_b \tag{11.46}$$

For the inverting amplifier shown in Figure 11.5, if we substitute Equation (11.43) into Equation (11.35), we get a closed-loop gain

$$\frac{V_O}{V_{IN}}(s) = -\frac{R_2/R_1}{1 + \left(1 + R_2/R_1\right)/A_o + \dfrac{s}{w_t/\left(1 + R_2/R_1\right)}} \tag{11.47}$$

In the case of non-inverting amplifier shown in Figure 11.12, if we substitute Equation (11.43) into Equation (11.37), we get the closed-loop gain expression

$$\frac{V_O}{V_{IN}}(s) = \frac{1 + R_2/R_1}{1 + \left(1 + R_2/R_1\right)/A_o + \dfrac{s}{w_t/\left(1 + R_2/R_1\right)}} \tag{11.48}$$

From Equations (11.47) and (11.48), it can be seen that the break frequency for the inverting and non-inverting amplifiers is given by the expression

$$w_{3dB} = \frac{w_t}{1 + R_2/R_1} \tag{11.49}$$

The following example illustrates the effect of the ratio $\frac{R_2}{R_1}$ on the frequency response of op amp circuits.

Example 11.5

An op amp has an open-loop dc gain of 10^7, the unity gain bandwidth of 10^8 Hz. For an op amp connected in an inverting configuration (Figure 11.5), plot the magnitude response of the closed-loop gain.
if $\frac{R_2}{R_1}$ = 100 , 600, 1100

Solution

Equation (11.47) can be written as

$$\frac{V_o}{V_{IN}}(s) = \frac{\dfrac{w_t R_2}{R_1(1 + R_2/R_1)}}{s + \dfrac{w_t}{A_0} + \dfrac{w_t}{(1 + R_2/R_1)}} \tag{11.50}$$

MATLAB script

```
% Inverter closed-loop gain versus frequency
w = logspace(-2,10);    f = w/(2*pi);
r12 = [100 600 1100];
```

```
a =[];    b = [];   num = [];   den = [];  h = [];
for i = 1:3
 a(i) = 2*pi*1.0e8*r12(i)/(1+r12(i));
 b(i) = 2*pi*1.0e8*((1/(1+r12(i))) + 1.0e-7);
 num = [a(i)];
 den = [1 b(i)];
 h(i,:) = freqs(num,den,w);
end
semilogx(f,abs(h(1,:)),'w',f,abs(h(2,:)),'w',f,abs(h(3,:)),'w')
title('Op Amp Frequency Characteristics')
xlabel('Frequency, Hz')
ylabel('Gain')
axis([1.0e-2,1.0e10,0,1200])
text(1.5e-2, 150, 'Resistance ratio of 100')
text(1.5e-2, 650, 'Resistance ratio of 600')
text(1.50e-2, 1050, 'Resistance ratio of 1100')
```

Figure 11.19 shows the plots obtained from the MATLAB program.

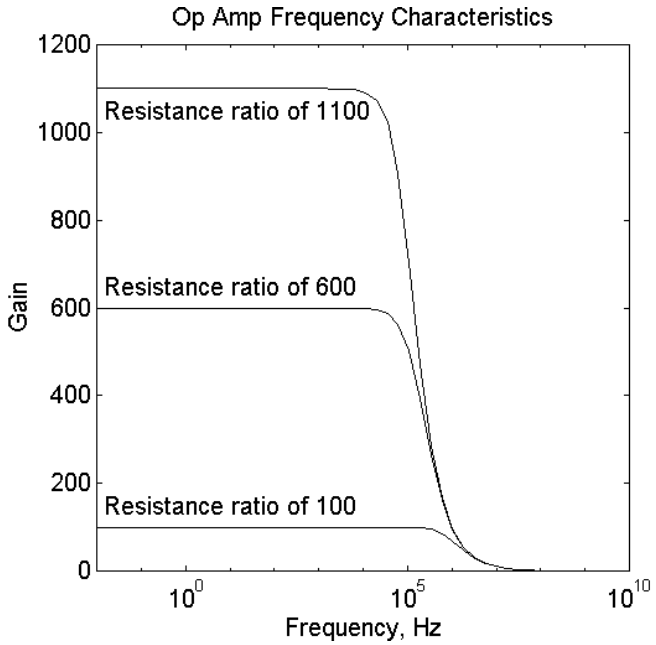


Figure 11.19 Frequency Response of an Op Amp Inverter with Different Closed Loop Gain

11.6 SLEW RATE AND FULL-POWER BANDWIDTH

Slew rate *(SR*) is a measure of the maximum possible rate of change of the output voltage of an op amp. Mathematically, it is defined as

$$SR = \left.\frac{dV_O}{dt}\right|_{\max} \tag{11.51}$$

The slew rate is often specified on the op amp data sheets in V/μs. Poor op amps might have slew rates around 1V/μs and good ones might have slew rates up to 1000 V/μs are available, but the good ones are relatively expensive.

Slew rate is important when an output signal must follow a large input signal that is rapidly changing. If the slew rate is lower than the rate of change of the input signal, then the output voltage will be distorted. The output voltage will become triangular, and attenuated. However, if the slew rate is higher than the rate of change of the input signal, no distortion occurs and input and output of the op amp circuit will have similar wave shapes.

As mentioned in the Section (11.5), frequency compensated op amp has an internal capacitance that is used to produce a dominant pole. In addition, the op amp has a limited output current capability, due to the saturation of the input stage. If we designate $I_{\max}$ as the maximum possible current that is available to charge the internal capacitance of an op amp, the charge on the frequency-compensation capacitor is

$$CdV = Idt$$

Thus, the highest possible rate of change of the output voltage is

$$SR = \left.\frac{dV_O}{dt}\right|_{\max} = \frac{I_{\max}}{C} \tag{11.52}$$

For a sinusoidal input signal given by

$$v_i(t) = V_m \sin wt \tag{11.53}$$

The rate of change of the input signal is

$$\frac{dv_i(t)}{dt} = wV_m \cos wt \tag{11.54}$$

Assuming that the input signal is applied to a unity gain follower, then the output rate of change

$$\frac{dV_O}{dt} = \frac{dv_i(t)}{dt} = wV_m \cos wt \tag{11.55}$$

The maximum value of the rate of change of the output voltage occurs when $\cos(wt) = 1$, i.e., $wt = 0, 2\pi, 4\pi. \ldots,$ the slew rate

$$SR = \left.\frac{dV_O}{dt}\right|_{\max} = wV_m \tag{11.56}$$

Equation (11.56) can be used to define full-power bandwidth. The latter is the frequency at which a sinusoidal rated output signal begins to show distortion due to slew rate limiting. Thus

$$w_m V_{o,rated} = SR \tag{11.57}$$

Thus

$$f_m = \frac{SR}{2\pi, V_{o,rated}} \tag{11.58}$$

The full-power bandwidth can be traded for output rated voltage, thus, if the output rated voltage is reduced, the full-power bandwidth increases. The following example illustrates the relationship between the rated output voltage and the full-power bandwidth.

Example 11.6

The LM 741 op amp has a slew rate of 0.5 V/μs. Plot the full-power bandwidth versus the rated output voltage if the latter varies from ± 1 to ± 10 V.

Solution

```
% Slew rate and full-power bandwidth

sr = 0.5e6;
```

```
v0 = 1.0:10;
fm = sr./(2*pi*v0);

plot(v0,fm)
title('Full-power Bandwidth vs. Rated Output Voltage')
xlabel('Rated output voltage, V')
ylabel('Bandwidth, Hz')
```

Figure 11.20 shows the plot for Example 11.6.

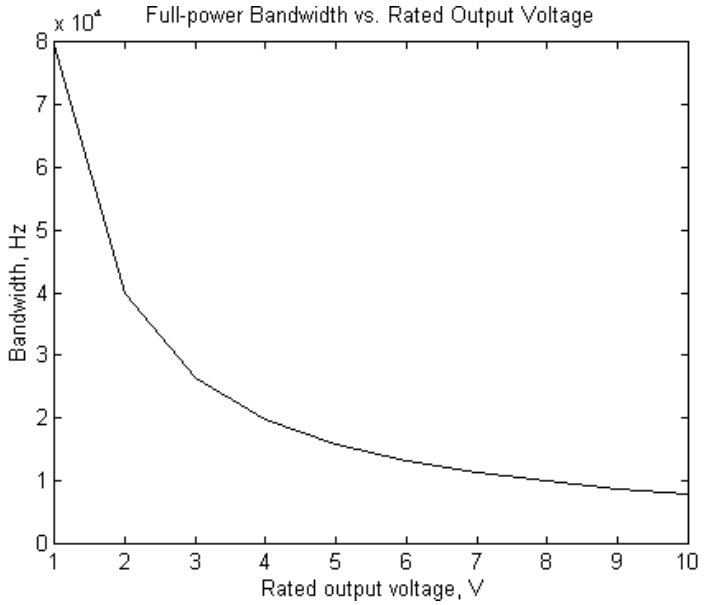
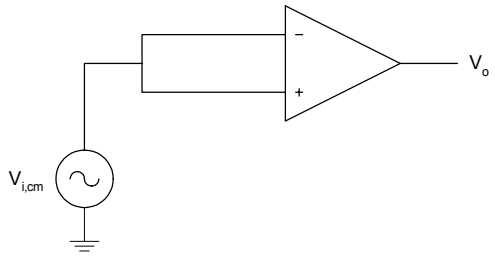


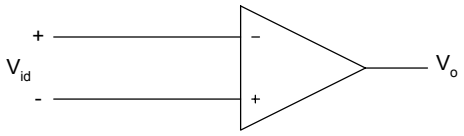
Figure 11.20 Rated Output Voltage versus Full-power Bandwidth

11.7 COMMON-MODE REJECTION

For practical op amps, when two inputs are tied together and a signal applied to the two inputs, the output will be nonzero. This is illustrated in Figure 11.21a, where the



(a)



(b)

Figure 11.21 Circuits Showing the Definitions of (a) Common-mode Gain and (b) Differential-mode Gain

common-mode gain, A_{cm}, is defined as

$$A_{cm} = \frac{v_o}{v_{i,cm}} \tag{11.59}$$

The differential-mode gain, A_d, is defined as

$$A_d = \frac{v_o}{v_{id}} \tag{11.60}$$

For an op amp with arbitrary input voltages, V_1 and V_2 (see Figure 11.21b), the differential input signal, v_{id}, is

$$v_{id} = V_2 - V_1 \tag{11.61}$$

and the common mode input voltage is the average of the two input signals,

$$V_{i,cm} = \frac{V_2 + V_1}{2} \tag{11.62}$$

The output of the op amp can be expressed as

$$V_O = A_d v_{id} + A_{cm} v_{i,cm} \tag{11.63}$$

The common-mode rejection ratio (CMRR) is defined as

$$CMRR = \left| \frac{A_d}{A_{cm}} \right| \tag{11.64}$$

The CMRR represents the op amp's ability to reject signals that are common to the two inputs of an op amp. Typical values of CMRR range from 80 to 120 dB. CMRR decreases as frequency increases.

For an inverting amplifier as shown in Figure 11.5, because the non-inverting input is grounded, the inverting input will also be approximately 0 V due to the virtual short circuit that exists in the amplifier. Thus, the common-mode input voltage is approximately zero and Equation (11.63) becomes

$$V_O \cong A_d V_{id} \tag{11.65}$$

The finite CMRR does not affect the operation of the inverting amplifier.

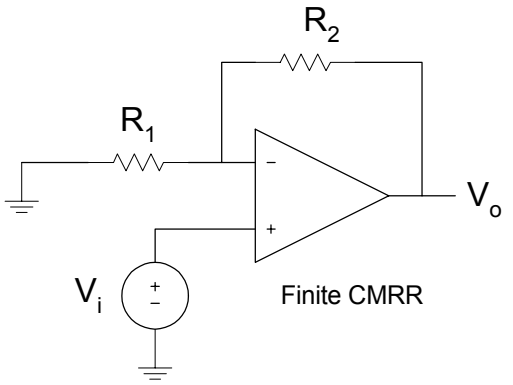
A method normally used to take into account the effect of finite CMRR in calculating the closed-loop gain is as follows: The contribution of the output voltage due to the common-mode input is $A_{cm} V_{i,cm}$. This output voltage contribution can be obtained if a differential input signal, V_{error}, is applied to the input of an op amp with zero common-mode gain.

Thus

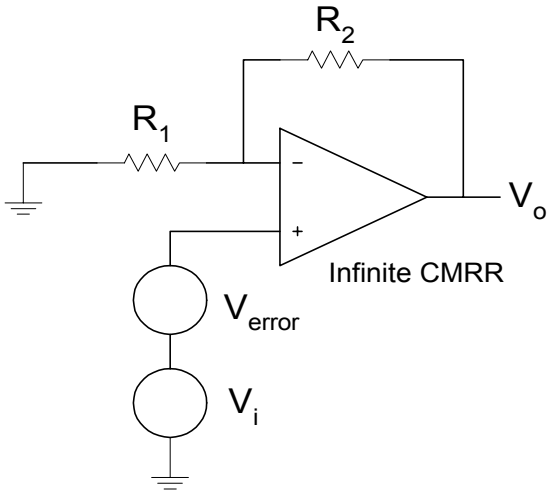
$$V_{error} A_d = A_{cm} V_{i,cm} \tag{11.66}$$

$$V_{error} = \frac{A_{cm} V_{i,cm}}{A_d} = \frac{V_{i,cm}}{CMRR} \tag{11.67}$$

Figure 11.22 shows how to use the above technique to analyze a non-inverting amplifier with a finite CMRR.



(a)



(b)

Figure 11.22 Non-inverting Amplifier (a) Finite CMRR (b) Infinite CMRR

From Figure 11.22b, the output voltage is given as

$$V_O = V_i\left(1 + R_2/R_1\right) + \frac{V_i}{CMRR}\left(1 + R_2/R_1\right) \tag{11.68}$$

The following example illustrates the effect of a finite CMRR on the closed-loop gain of a non-inverting amplifier.

Example 11.7

For the amplifier shown in Figure 11.22, if R_2 = 50KΩ and R_1 = 1KΩ, plot the closed-loop gain versus CMRR for the following values of the latter: $10^4, 10^5, 10^6, 10^7, 10^8$ and 10^9.

Solution

MATLAB Script

```
% Non-inverting amplifier with finite CMRR
r2 = 50e3; r1 = 1.0e3; rr = r2/r1;
cmrr = logspace(4,9,6);  gain = (1+rr)*(1+1./cmrr);
semilogx(cmrr,gain,'wo')
xlabel('Common-mode Rejection Ratio')
ylabel('Closed Loop Gain')
title('Gain versus CMRR')
axis([1.0e3,1.0e10,50.998, 51.008])
```

Figure 11.23 shows the effect of CMRR on the closed loop of a non-inverting amplifier.

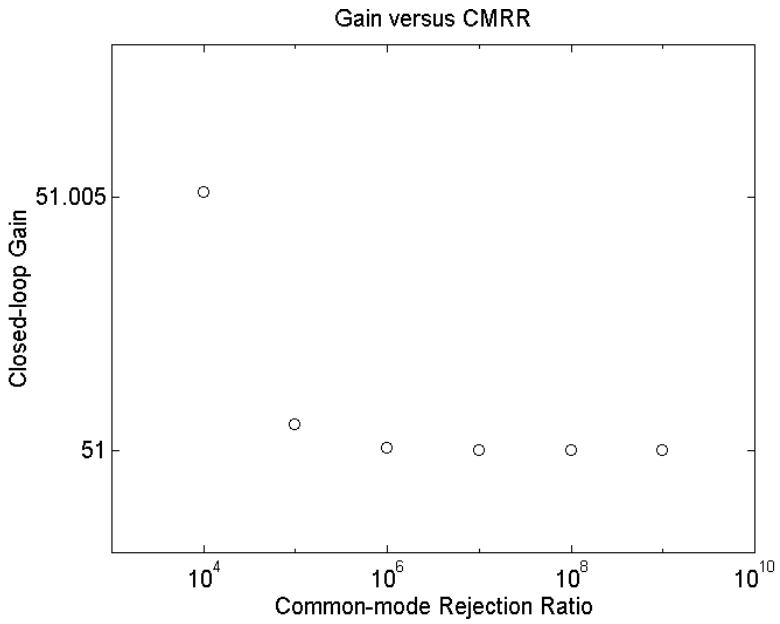


Figure 11.23 Effect of finite CMRR on the Gain of a Non-inverting Amplifier

SELECTED BIBLIOGRAPHY

1. Schilling, D.L. and Belove, C., *Electronic Circuits - Discrete and Integrated*, 3rd Edition, McGraw Hill, 1989.

2. Wait, J.V., Huelsman, L.P., and Korn, G.A., *Introduction to Operational Amplifiers - Theory and Applications*, 2nd Edition, McGraw Hill, 1992.

3. Sedra, A.S. and Smith, K.C., *Microelectronics Circuits*, 4th Edition, Oxford University Press, 1997.

4. Ferris, C.D., *Elements of Electronic Design*, West Publishing, 1995.

5. Irvine, R.G., *Operational Amplifiers - Characteristics and Applications*, Prentice Hall, 1981.

6. Ghausi, M.S., *Electronic Devices and Circuits: Discrete and Integrated*, HRW, 1985.

EXERCISES

11.1 For the circuit shown in Figure P11.1, (a) derive the transfer function $\frac{V_O}{V_{IN}}(s)$. (b) If R_1 = 1KΩ, obtain the magnitude response.

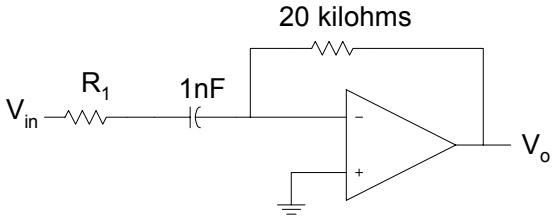


Figure P11.1 An Op Amp Filter

11.2 For Figure 11.12, if the open-loop gain is finite, (a) show that the closed-loop gain is given by the expression shown in Equation (11.37). (b) If R_2 = 100K and R_1 = 0.5K, plot the percentage error

in the magnitude of the closed-loop gain for open-loop gains of $10^2, 10^4, 10^6$ and 10^8.

11.3 Find the poles and zeros of the circuit shown in Figure P11.3. Use MATLAB to plot the magnitude response. The resistance values are in kilohms.

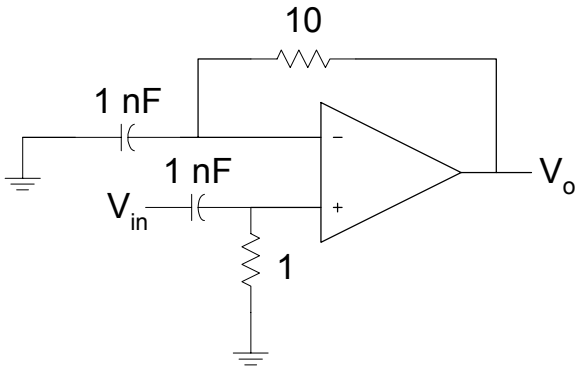


Figure P11.3 An Op Amp Circuit

11.4 For the amplifier shown in Figure 11.12, if the open-loop gain is 106, R_2 = 24K, and R_1 = 1K, plot the frequency response for a unity gain bandwidth of $10^6, 10^7$, and 10^8 Hz.

11.5 For the inverting amplifier, shown in Figure 11.5, plot the 3-dB frequency versus resistance ratio $\frac{R_2}{R_1}$ for the following values of the resistance ratio: 10, 100, 1000, 10,000 and 100,000. Assume that $A_O = 10^6$ and $f_t = 10^7$ Hz.

11.6 For the inverting amplifier, shown in Figure 11.5, plot the closed loop gain versus resistance ratio $\frac{R_2}{R_1}$ for the following open-loop gain, A_O: 103, 105 and 107. Assume a unity gain bandwidth of

$f_t = 10^7$ Hz and resistance ratio, $\frac{R_2}{R_1}$ has the following values: 10, 100, 1000, 10,000 and 100,000.

11.7 An op amp with a slew rate of 1 V/μs is connected in the unity gain follower configuration. A square wave of zero dc voltage and a peak voltage of 1 V and a frequency of 100 KHz is connected to the input of the unity gain follower. Write a MATLAB program to plot the output voltage of the amplifier.

11.8 For the non-inverting amplifier, if R_{icm} = 400 MΩ, R_{id} = 50 MΩ, R_1 = 2KΩ and R_2 = 30KΩ, plot the input resistance versus the dc open-loop gain A_0. Assume the following values of the open-loop gain: $10^3, 10^5, 10^7$ and 10^9.